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Quantum Computer in the Solid State

AdMOS GmbH: QSolid_KryoMod - Simulation Models for Highly Integrated Cryogenic Electronics

Modeling Approach

- The aim of the project is to generate a simulation library which covers the temperature range from 298 K (room temperature) down to 4 K or less and provide it to the partners in WP5.2 to support circuit design.
- Base is BSIM-IMG 102-9.6 model with built-in cryogenic extension.
- Model parameters were calibrated to align simulation behavior with the observed characteristics across the temperature range.
- Library was verified on device and circuit level.

A. SPICE MODELS FOR CRYOGENIC APPLICATIONS

MOS simulation models for bulk or SOI devices are:

- designed to cover typically temperatures between 200 °C (398 K) to -55 °C (218 K) for applications like automotive electronics.
- models can alternatively be adjusted to one temperature (e.g. 4 K for helium-cooled circuits) but need to keep simulation temperature Temp=25, despite the actual temperature being, for example, 4 K.
- MOS models could encounter inconsistencies or errors in their formulation or mathematical approximations as temperatures approaches T = 0 K.
- Standard models for FDSOI transistors (BSIM-IMG 102.9.4, LUTSOI 102.5) failed below approximately 40 K.

BSIM-IMG 102.9.6 model released 2023 from UC Berkeley with a new cryogenic extension could successfully be applied. It is publicly available and is implemented in the design environments for integrated circuits.

B. MODEL PARAMETER EXTRACTION

Modify existing library from project partner Global Foundries (GF) for FDSOI 22 nm SLVT PMOS and NMOS transistors. Extension of each model parameter to accommodate the cryogenic range:

kt1 = kt1ext + kt1qsolid (1)

kt1: effective model parameter
kt1ext: the parameter from available foundry library
kt1qsolid: additional term accounting for the cryogenic temperature.

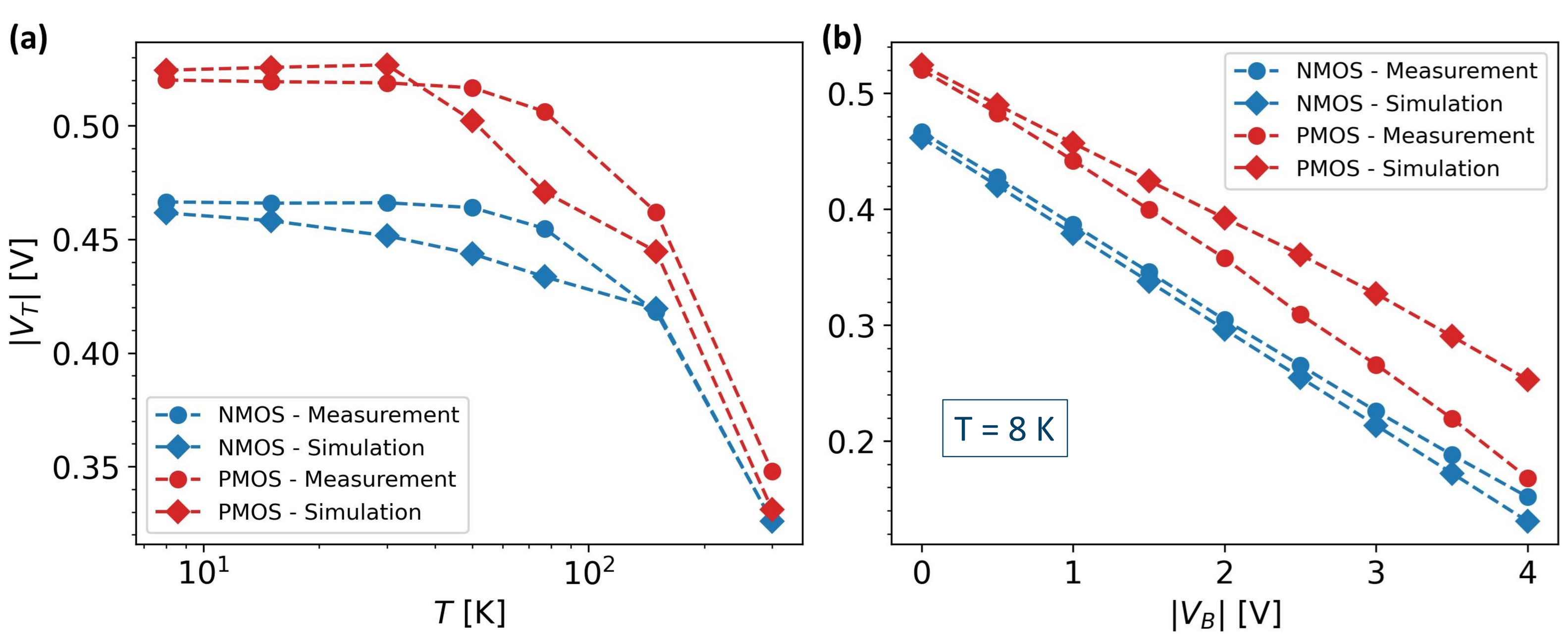
Newly added parameters to BSIM-IMG 102.9.6.:

kt11 = 0.01 + kt11qsolid (2)

Example: adjustment of threshold voltage versus temperature at different back bias values applying model parameters kt11 and kt12 (correlated to Vth) from cryogenic extension.

C. DEVICE-LEVEL VALIDATION

THRESHOLD VOLTAGE

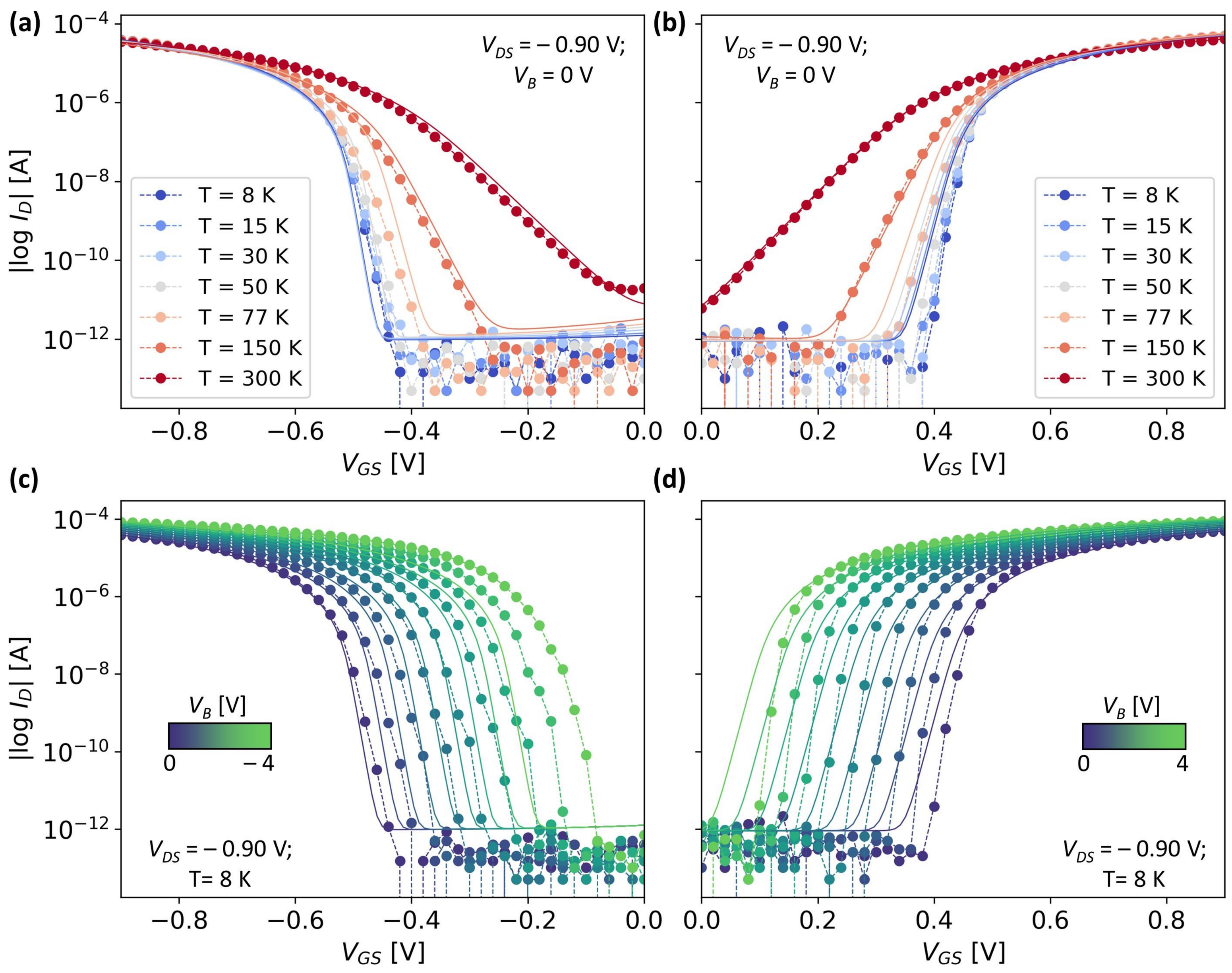


Threshold voltage values were extracted using the constant current method for all measured and simulated curves.

Figure above shows the extracted threshold voltage values of the I-V curves plotted together against temperature (a). For both PMOS and NMOS transistors, the values increase with decreasing temperature and start to saturate towards lower temperatures around 30 K.

The back-bias voltage dependency |VB| is shown in (b) for T = 8 K.

I-V CURVES



Measured (symbols) and simulated (lines) transfer curves at different temperatures for short-channel (a) PMOS and (b) NMOS transistor; Measured and simulated transfer curves at 8 K for different back-bias voltages (c) PMOS and (d) NMOS transistor:

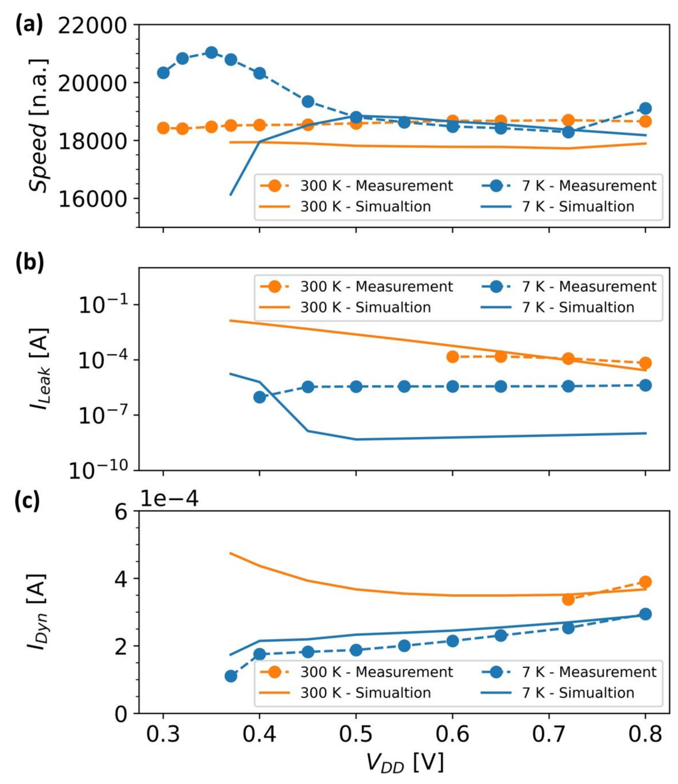
- Good match to the measurements at room temperature.
- Cryogenic temperatures: larger deviation from measurement points specially at high |VB| values in weak inversion and subthreshold region.

D. CIRCUIT-LEVEL VALIDATION

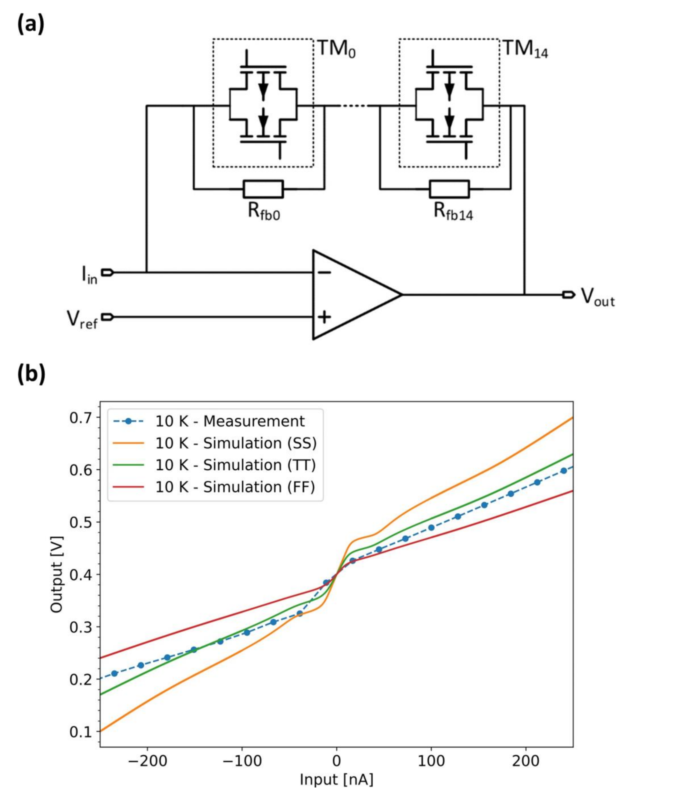
AdMOS' partners in the QSolid WP5.2, Raycics GmbH and FZ Jülich ZEA-2, provided 2 kind of test chips and performed the verification:

- Different ring oscillators with adaptive back biasing (ABB) or standard cell design (Raycics GmbH).
- Transimpedance amplifier (ZEA-2).

Both test chips were produced by Global Foundries using the SLVT variants of the FDSOI22 transistors.



Standard Cell Ring oscillator



Transimpedance amplifier

E. Next Steps to Improve Model to Hardware Correlation

- Model refinement based on an extended set of measured data from project partners with focus on back-bias voltage and dynamic behavior.
- Provide in addition extended simulation models of diodes and passives in cryogenic temperature range to designers.

AdMOS GmbH Advanced Modeling Solutions
In den Gernäckern 8
72636 Frickenhausen/Germany
https://admos.de, info@admos.de
+49 7025 911698-0

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